REMARKS

Claims 1, 7, 11, and 12 are currently pending in the present application, with Claims 1 and 11 being amended. Reconsideration and reexamination of the claims are respectfully requested.

The Examiner objected to the disclosure due to various informalities. Applicants have amended the specification to correct the informalities. However, with respect to the description of reference label 50 for Figs. 3 and 5, Applicants direct the Examiner's attention to page 4, line 23, and page 6, line 20, wherein the reference label 50 in Figs. 3 and 5 are respectively described as conductive fillings for vias 22. With respect to reference labels 16, 16' and 16" relative to Fig. 5, Applicants point the Examiner to Page 6, lines 4-6 of the specification, in which the labels are described.

The Examiner objected to the drawings due to certain informality. More specifically, the Examiner indicated that label 10 still needs to be added to the drawing. Applicants respectfully disagrees with the Examiner in that conductive layers 10, which are separated by nonconductive separator layers 20, are not shown in Fig. 6. Rather, Fig. 6 shows the arrangements of the conductive strips (16', 16'', and 16''') and the vias 22. Accordingly, label 10 should not be added to Fig. 6.

The Examiner objected to the claims due to certain informalities. More specifically, the Examiner suggested that "form" and "forming" should be rewritten as --provide-- and --providing--, respectively. Applicants have amended the claims accordingly.

The Examiner rejected Claims 1 and 7 under 35 U.S.C. § 102(b) as being anticipated by Landis. This rejection is respectfully traversed with respect to the amended claims.

Claims 1 and 7 are directed to an integrated chip having an on-chip transmission line, whereby the monolithic transmission line includes multiple layers of alternating conductive layers and nonconductive layers, and whereby the top and bottom conductive layers have a uniform distance from each other, and substantially equals to the distance between the two laterally spaced terminal conductive strips.

Landis does not remotely show or suggest an integrated chip having an on-chip monolithic transmission line. Applicants disagree with the Examiner in that Figs. 1 and 3 do not show an on-chip embedded transmission line. Rather, Figs. 1 and 3 simply show conductive strips that are embedded on a circuit board whereby chips mounted on the boards can be connected to each other via the board-embedded transmission lines via wires 64 and 66. Although Fig. 3 shows two integrated circuit chips, Landis simply does not show the chips as having on-chip transmission lines. As the Examiner is well aware, the difference between a circuit board and an integrated circuit is fundamental in that a circuit board is simply comprised of various conductive structures, while an integrated circuit is comprised of various circuit elements. Claims 1 and 7 is specifically directed to an integrated chip having an on-chip transmission line. This is clearly not shown in Landis. Accordingly, Applicants respectfully submit that Claims 1 and 7 are not anticipated by, nor obvious in view of, Landis.

The Examiner rejected Claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Landis. This rejection is respectfully traversed with respect to the amended claim.

Similar to arguments made above, Claim 11 is directed to an integrated chip having an on-chip transmission line. Landis simply does not contain any disclosure or suggestion of an integrated chip having on-chip transmission lines. Rather, Landis is simply directed to isolating transmission lines within a circuit board. In fact, by showing the chips on a circuit board connected via wires, Fig. 3 of Landis make obvious that Landis is not directed to on-chip transmission lines. Accordingly, Applicants respectfully submit that Claims 11 is not obvious in view of Landis.

The Examiner objected to Claim 12 but did not specifically detail the reasons for the objection. Applicants assume that the objection was based on the informalities contained in the base claim, and that Claim 12 is now in condition for allowance in view of the amendments made to Claim 11.

In view of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. An entry of the claim amendments after final is requested.

Reconsideration and reexamination of the claims and an early allowance is solicited. If the Examiner believes it would further advance the prosecution of the present application, he is respectfully requested to contact the undersigned attorney.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant(s) petition(s) for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 53535.20005.00.

Respectfully submitted,

Dated: April 17, 2003

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On Page 3, the Paragraph starting at line 25 and ending at line 28 has been amended in the following manner:

Figs. 1 and 2 depict elevational section views of the prior art [strip] microstrip line 1 and [microstrip monolithic 5 constructions] strip line 5 monolithic constructions respectively. Both of these constructions are well known in the planar fabrication and microcircuit technology. In Fig. 1, the strip line comprises a metal conductor 2 etched on top of an insulator 4, which in turn rests on a layer of conductor 3.

On Page 3, the Paragraph starting at line 30 and ending at Page 4, line 2 has been amended in the following manner:

The [microstrip] stripline construction 5 shown in Fig. 2 comprises a pair of metal conductors 6 and 8 in spaced apart positions with one of the conductors 9 embedded within the insulation material 7. In both of these constructions, the only way to achieve field isolation is to space adjacent conductors apart. However, this uses an undesirable amount of surface area on the substrate to achieve such isolation.

On Page 5, the Paragraph starting at line 13 has been amended in the following manner:

Each of the other of the conductive layers 10 between the one of the conductive layers 16 and the top one of the conductive planes 14, and between the one of the conductive layers 16 and the bottom one of the conductive planes 12, comprises a pair of laterally spaced apart conductive strips separated by a nonconductive spacer layer 42 so that the pair of laterally spaced conductive strips are spaced approximately at the selected width, i.e., the stack width 32. Each of the nonconductive separator layers 20 provides a plurality of [metal filled] vias 22 filled with conductive material 50 conductively joining the two outermost 16', 16''' of the three conductive strips of the one of the conductive layers 16, and the spaced apart conductive strips of the other of the conductive layers 10, and the conductive planes 12, 14 so as to form a conductive sidewall shield about the centermost 16" of the three laterally spaced apart conductive strips.

On Page 7, the Paragraph starting at line 13 has been amended in the following manner:

The process further comprises the step of extending, by simple metal deposition, the initial 12 and the final 14 ones of [said] conductive layers, as the top and the bottom conductive planes, to define the mutually registered selected width 32 of the stack 30.

In the Claims:

Claims 1 and 11 have been amended in the following manner:

1. (Twice amended) [A] An integrated circuit chip having an on-chip multi-layer metal-shielded monolithic transmission line comprising:

a plurality of parallel planar thin film conductive layers; and

a plurality of planar thin film nonconductive separator layers disposed such that each adjacent pair of the conductive layers is separated by at least one of said plurality of planar thin film nonconductive layers to [form] provide a stack of alternating conductive and nonconductive layers,

wherein an initial one and a final one of said conductive layers [form] provide a top conductive plane and a bottom conductive plane,

wherein a center one of the conductive layers comprises three laterally spaced apart conductive strips, said conductive strips separated by nonconductive material such that two laterally spaced terminal strips of the three conductive strips are spaced at a selected width from the center conductive strip,

wherein each of the nonconductive separator layers include a plurality of vias between the two laterally spaced terminal conductive strips of the three conductive strips and the top and bottom conductive planes, said plurality of vias filled with conductive material, and

wherein the distance between the top and bottom conductive planes is substantially equal to the distance between the two laterally spaced terminal conductive strips.

11. (Twice amended) [A] An integrated circuit chip having a plurality of on-chip multi-layer metal-shielded monolithic transmission lines comprising:

a plurality of parallel planar thin film conductive layers, each adjacent pair of the conductive layers separated by at least one of a plurality of planar thin film nonconductive separator layers to [form] provide a stack of alternating conductive and nonconductive said layers,

wherein an initial one and a final one of said conductive layers [forming] providing a top conductive plane and a bottom conductive plane,

wherein one of the conductive layers between the top and the bottom conductive planes includes a plurality of N laterally spaced apart conductive strips, where N is an odd integer,

wherein each laterally adjacent pair of the conductive strips are separated at a predetermined width by nonconductive material,

wherein the plurality of nonconductive separator layers include a plurality of metal filled vias positioned for electrically interconnecting every other one of the laterally spaced apart conductive strips to the top an bottom conductive planes, and

wherein the distance between top conductive plane and bottom conductive plane is substantially equal to the distance between every other laterally spaced conductive strips .